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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,475	07/18/2002	Wang-Jin Chen	FTCP0003USA	7907

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MERRIFIELD, VA 22116

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,475	CHEN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,4,5 and 7 is/are rejected.

7)☒ Claim(s) 2,3,6 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 July 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7 are presented for examination.

Allowable Subject Matter

Claims 2, 3, and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li U. S. Patent No. 6,023,778.

As per claim 1, Li substantially teaches the claimed invention using a delay circuit to act as a buffer for the scan enable signal received by the mux scan flip-flops of a test circuit. Thus, instead of a scan mode signal being sent directly to each mux scan flip-flop, the scan mode signal is first sent to the delay circuit, which then distributes the scan mode signal to the mux scan flip-flops. Since each delay circuit can serve as the buffer for numerous mux scan flip-flops, the scan mode signal is sent initially to a smaller number of delay circuits instead of the thousands of mux scan flip-flops that may be distributed throughout the entire integrated circuit. The described delay circuit synchronizes a system clock cycle with the active-to-inactive transition of the scan mode signal, thereby enabling the mux scan flip-flops to be loaded and unloaded with test data at slower scan speed, and allowing the integrated circuit to be operated at full system speed to detect speed-related defects (column 3 lines 36-54, column 4 lines 14-31 and figures 4A and 4B). Not explicitly disclosed is that the delay circuit is internal to the multiplexer. However, it would have been obvious to a person having ordinary

skill in the art at the time this invention was made to have placed the delay circuit in the path of the incoming test data whether internal or external to the multiplexer circuit. This would have been obvious as suggested by Li by utilizing mux scan flip-flops to test for speed-related defects in integrated circuits (column 2 lines 40-43).

As per claim 4, Li teaches a delay circuit is used to act as a buffer for a scan enable signal received by the mux scan flip-flops of a test circuit. Abstract

Claims 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li U. S. Patent No. 6,023,778 as applied to claims 1 above, and further in view of Srinivasan et al. U.S. Patent No. 6,698,006.

As per claims 5 and 7, Li substantially teaches the claimed invention using a delay circuit to act as a buffer for the scan enable signal received by the mux scan flip-flops of a test circuit. Thus, instead of a scan mode signal being sent directly to each mux scan flip-flop, the scan mode signal is first sent to the delay circuit, which then distributes the scan mode signal to the mux scan flip-flops. Since each delay circuit can serve as the buffer for numerous mux scan flip-flops, the scan mode signal is sent initially to a smaller number of delay circuits instead of the thousands of mux scan flip-flops that may be distributed throughout the entire integrated circuit. The described delay circuit synchronizes a system clock cycle with the active-to-inactive transition of the scan mode signal, thereby enabling the mux scan flip-flops to be loaded and unloaded with test data at slower scan speed, and allowing the integrated circuit to be

operated at full system speed to detect speed-related defects (column 3 lines 36-54, column 4 lines 14-31 and figures 4A and 4B). Not explicitly disclosed is the use of RC or wire delay.

However, in an analogous art, Srinivasan et al. teach using wire length as a method of delay (column 21 lines 28-32), and also various aspects of using an RC model for delay in circuits (column 28 lines 23-35). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the scan multiplexer circuit with a delay of Li as discussed above with reference to claim 1, by using various methods of designing the delay circuit. This combination would have been obvious as suggested by Srinivasan et al. in order to correct timing violations (column 1 line 66 through column 2 line 4).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 5,923,676 Sunter et al.

This patent teaches a built-in self-test (BIST) for integrated circuits (ICs) and for systems including multiple ICs, measures signal propagation delays in combinational and sequential logic, set-up and hold times, and tri-state enable/disable times, from any circuit node to any other circuit node including pin-to-pin and from one IC to another. During test, an oscillator is created including the test bus, a constant delay, counters, and a delay path of interest or a reference path. The delay path of interest may include

e.g. an analog filter. A delay copier copies the delay between any two signal events, without injecting any test signal into the circuit under test (e.g. on-line test), and the delay copy can be measured by selecting it in the oscillator.

"*Cost-free Scan: A Low-Overhead Scan Path Design*" by Lin et al. in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, September 1998, page(s): 852 – 861, Volume 17 Issue 9, Inspec Accession Number: 6041731

This paper teaches that since conventional scan design imposes considerable area and delay overheads. To establish a scan chain in the test mode, multiplexers at the inputs of flip-flops and scan wires are added to the actual design. However, the functionality of the functional logic has not been utilized for the test purposes. A proposed low-overhead scan design methodology, called cost-free scan, which exploits the controllability of primary inputs to establish scan paths through the functional logic. It is shown how to analyze the circuit to determine all the free-scan flip-flops and select the best input vector to establish the maximum number of free-scan flip-flops for the scan chain design. In full-scan designs, as many as 89% of the flip-flops are found free-scannable. In the partial-scan designs, assuming that selecting flip-flops for scan to break sequential cycles is used to increase circuit testability; Reduction can be as high as 97% in scan flip-flops needed to break sequential cycles.

"*Test-Point Insertion: Scan Paths Through Functional Logic*" by Lin et al. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Sept. 1998, pages 838 – 851, Volume 17 Issue 9, Inspec Accession Number: 6041730

This paper teaches that conventional scan design imposes considerable area and delay overheads. To establish a scan chain in the test mode, multiplexers at the inputs of flip-flops and scan wires are added to the actual design. We propose a low-overhead scan design methodology that employs a new test-point insertion technique. Unlike the conventional test-point insertion, where test points are used directly to increase the controllability and observability of the selected signals, the test points are used here to establish scan paths through the functional logic. The proposed technique reuses the functional logic for scan operations; as a result, the design-for-testability overhead on area or timing can be minimized. We show an algorithm that uses the new test-point insertion technique to reduce the area overhead for the full-scan design. We also discuss its application to the timing-driven partial-scan design.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

Cynthia Britt
Examiner
Art Unit 2133

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